GLOMORE

GM-M-043WQ-AC1-L-4

LCD

4.3 Inch TFT LCD
With
Touch Screen Panel

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1. Revision History

DATE	VERSION	REVISED PAGE NO.	Note
2011/11/28	1		First issue
2012/08/30	2	4	Add Gray Scale Inversion Direction.

2. General Specification

This product is composed of a TFT LCD panel, driver ICs, FPC, Control Board and a backlight unit. The following table described the features of GM-M-043WQ-AC1-L-4

- Dot Matrix: 480(RGB) x272
- Module dimension: 105.5x 67.2 x 7.8 mm3
- View area: 95.04x 53.85 mm2
- Dot pitch: 0.066 x 0.198 mm2
- LCD type: TFT, Negative, Transmissive
- View direction: 12o'clock
- Gray Scale Inversion Direction: 6 o'clock
- Backlight Type: LED, Normally White

3. Interface Pin Function

3.1 Pins Connection To Control Board

P/N	Symbol	16BIT Function	P/N	Symbol	16BIT Function
1	GND	Ground	26	RST	Reset
2	VCC	Power supply for Logic	27	NC	No connection
3	BL_E	Backlight Enable	28	X1	Touch screen
4	RS		29	Y1	Touch screen
5	WR	8080 family MPU interface : Write signal	30	X2	Touch screen
6	RD	8080 family MPU interface: Read signal	31	Y2	Touch screen
7	DB0	Data bus	32	DISP	DISPLAY ON(1) / OFF(0)
8	DB1				
9	DB2				
10	DB3				
11	DB4				
12	DB5				
13	DB6				
14	DB7				
15	DB8				
16	DB9				
17	DB10				
18	DB11				
19	DB12				
20	DB13				
21	DB14				
22	DB15				
23	NC	No connection			
24	NC	No connection			
25	CS	Chip select			

4. Outline Dimension & Block Diagram

PIN NO.	SYMBOL	PIN NO.	SYMBOL
1	GND	18	DB11
2	VCC	19	DB12
3	[illegible]	20	DB13
4	RS	21	DB14
5	WR	22	DB15
6	RD	23	NC
7	DB0	24	NC
8	DB1	25	CS
9	DB2		
10	DB3		
11	DB4		
12	DB5		
13	DB6		
14	DB7		
15	DB8		
16	DB9		
17	DB10		

The non-specified tolerance of dimension is ±0.2mm.

LED BACKLIGHT
A
K
TFT PANEL
480(R.G.B)X272
(PANEL)
VDD
RBG 6/6/6
,EN,CLK,DISP
output 27.9V
/20mA
Backlight
circuit
TFT Controller
Control-Board
Y2
X2
Y1
X1
GND
VDD
B/L Enable
RS
WR
RD
CS
RES
DISP ON
8 Bits Data Bus
16 Bits Data Bus

5. DC CHARACTERISTICS

Conditions:

Voltage referenced to VSS

VDDD, VDDPLL = 1.2V

VDDIO, VDDLCD = 3.3V

TA = 25°C

DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
PSTY	Quiescent Power			300	500	uW
IIZ	Input leakage current		-1		1	uA
IOZ	Output leakage current		-1		1	uA
VOH	Output high voltage		0.8VDDIO			V
VOL	Output low voltage				0.2VDDIO	V
VIH	Input high voltage		0.8VDDIO		VDDIO + 0.5	V
VIL	Input low voltage				0.2VDDIO	V

6. AC Characteristics

Conditions:

Voltage referenced to VSS

VDDD, VDDPLL = 1.2V

VDDIO, VDDLCD = 3.3V

TA = 25°C

CL = 50pF (Bus/CPU Interface)

CL = 0pF (LCD Panel Interface)

6.1 Clock Timing

Table 6-1:Clock Input Requirements for CLK (PLL-bypass)

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)		110	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

Table 6-2:Clock Input Requirements for CLK

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)	2.5	50	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

Table 6-3:Clock Input Requirements for crystal oscillator XTAL

Symbol	Parameter	Min	Max	Units
FXTAL	Input Clock Frequency	2.5	10	MHz
TXTAL	Input Clock period	1/fXTAL		ns

6.2 MCU Interface Timing

6.2.1 Parallel 6800-series Interface Timing

Table 6-4: Parallel 6800-series Interface Timing Characteristics (Use CS# as clock)

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSH	Control Pulse High Width	Write Read	13 30	1.5* tMCLK 3.5* tMCLK	-	ns
tPWCSL	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	1.5* tMCLK 9* tMCLK 9* tMCLK	-	ns
tAS	Address Setup Time		2	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Data Setup Time		4	-	-	ns
tDHW	Data Hold Time		1	-	-	ns
tPLW	Write Low Time		14	-	-	ns
tPHW	Write High Time		14	-	-	ns
tPLWR	Read Low Time		38	-	-	ns
tACC	Data Access Time		32	-	-	ns
tDHR	Output Hold time		1	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-		0.5	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure 6-1: Parallel 6800-series Interface Timing Diagram (Use CS# as Clock)

Table 6-5: Parallel 6800-series Interface Timing Characteristics (Use E as clock)

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSH	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	1.5* tMCLK 9* tMCLK 9* tMCLK	-	ns
tPWCSL	Control Pulse High Width	Write Read	13 30	1.5* tMCLK 3.5* tMCLK	-	ns
tAS	Address Setup Time		2	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Data Setup Time		4	-	-	ns
tDHW	Data Hold Time		1	-	-	ns
tPLW	Write Low Time		14	-	-	ns
tPHW	Write High Time		14	-	-	ns
tPLWR	Read Low Time		38	-	-	ns
tACC	Data Access Time		32	-	-	ns
tDHR	Output Hold time		1	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure 6-2: Parallel 6800-series Interface Timing Diagram (Use E as Clock)

6.2.2 Parallel 8080-series Interface Timing

Table 6-6: Parallel 8080-series Interface

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSL	Control Pulse High Width	Write Read	13 30	1.5* tMCLK 3.5* tMCLK	-	ns
tPWCSH	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	1.5* tMCLK 9* tMCLK 9* tMCLK	-	ns
tAS	Address Setup Time		1	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Write Data Setup Time		4	-	-	ns
tDHW	Write Data Hold Time		1	-	-	ns
tPWLW	Write Low Time		12	-	-	ns
tDHR	Read Data Hold Time		1	-	-	ns
tACC	Access Time		32	-	-	ns
tPWLR	Read Low Time		36	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns
tCS	Chip select setup time		2	-	-	ns
tCSH	Chip select hold time to read signal		3	-	-	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure 6-3: Parallel 8080-series Interface Timing Diagram (Write Cycle)

Figure 6-4: Parallel 8080-series Interface Timing Diagram (Read Cycle)

7. Data transfer order Setting

Pixel Data Format

Both 6800 and 8080 support 8-bit, 9-bit, 16-bit, 18-bit and 24-bit data bus. Depending on the width of the data bus, the display data are packed into the data bus in different ways.

Table 7-1: Pixel Data Format

Interface	Cycle	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
24 bits	1st	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
18 bits	1st							R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16 bits (565 format)	1st									R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1
16 bits	1st									R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0
	2nd									B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0
	3rd									G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
12 bits	1st													R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4
	2nd													G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
9 bits	1st																R5	R4	R3	R2	R1	R0	G5	G4	G3
	2nd																G2	G1	G0	B5	B4	B3	B2	B1	B0
8 bits	1st																	R7	R6	R5	R4	R3	R2	R1	R0
	2nd																	G7	G6	G5	G4	G3	G2	G1	G0
	3rd																	B7	B6	B5	B4	B3	B2	B1	B0

8. Register Depiction

Please consult the spec of SSD1963 Version 1.2

9. OPTICAL CHARATERISTIC

Item	Symbol	Condition	Values			Unit	Remark
			Min.	Typ.	Max.		
Viewing angle (CR≧10)	L	=180^0(9 O' clock)	60	70	—	degree	Note1
	R	=0^0(3 O' clock)	60	70	—		
	T	=90^0(12 O' clock)	40	50	—		
	B	=270^0(6 O' clock)	60	70	—		
Response time	T_{ON}	Normal =0^0	—	10	20	msec	Note 3
	T_{OFF}			15	30	msec	Note 3
Contrast ratio	CR		400	500	—	—	Note 4
Color chromaticity	W_X		0.26	0.31	0.36	—	Note 2 Note 5 Note 6
	W_Y		0.28	0.33	0.38	—	
Luminance	L		350	400	—	Cd/m^2	Note 6
Luminance uniformity	Yu		70	75	—	%	Note 7

Note 1: Definition of viewing angle range

Fig. 4-1 Definition of viewing angle

Note 2: Definition of optical measurement system.
The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/Field of view: 1° /Height: 500mm.)

Fig. 4-2 Optical measurement system setup

Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

Fig. 4-3 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: All input terminals LCD panel must be ground while measuring the center area of the panel. The LED driving condition is I_L=20mA.

Note 7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer to Fig. 4-4).Every measuring point is placed at the center of each measuring area.

$$Luminance\ \ Uniformity\ (Yu) = \frac{B_{min}}{B_{max}}$$

L-------Active area length W----- Active area width

Fig. 4-4 Definition of measuring points

B_{max}: The measured maximum luminance of all measurement position.
B_{min}: The measured minimum luminance of all measurement position.

10. Electrical Characteristics

Item	Symbol	Values			Unit	Remark
		Min	TYP	max		
Operating voltage	VDD	3.1	3.3	3.5	V	
Input high voltage	VIH	0.8*VDD	-	VDD	V	
Input low voltage	VIL	0	-	0.2*VDD	V	
Output high voltage	VOH	VDD-0.3		VDD	V	
Output low voltage	VOL	0	-	0.3	V	
Current Consumption	IVCI	-	245	-	mA	
Power Consumption	PLCD	-	808.5	-	mW	

11.Absolute Maximum Ratings

Item	Symbol	Values		Unit	Remark
		Min	max		
Power Supply Voltages	VDD	-0.5	5.0	V	
Input signal voltage	Logic input	-0.5	5.0	V	
Operating Temperature	Topa	-20	70	◦ C	Note3,4
Storage Temperature	Tst	-30	80	◦ C	Note3,4
LED Reverse Voltage	Vr	-	1.2	V	Each LED Note2
LED Forward Current	IF	-	25	mA	Each LED
LED life time	--	20,000	--	--	Note5

Note 1: The absolute maximum rating values of this product are not allowed to be exceeded at any times. A module should be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme condition, the module may be permanently destroyed.

Note 2: VR Conditions: Zener Diode 20mA

Note 3: 90% RH Max. (Max wet temp. is 60℃)

Maximum wet-bulb temperature is at 60℃ or less. And No condensation (no drops of dew)

Note 4: In case of temperature below 0℃,the response time of liquid crystal (LC) becomes slower and the color of panel darker than normal one.

Note 5: The “LED life time” is defined as the module brightness decrease to 50% original brightness that the ambient temperature is 25℃ and IL =20mA. The LED lifetime could be decreased if operating IL is lager than 20 mA.

12. RELIABILITY TEST

WIDE TEMPERATURE RELIABILITY TEST

NO	ITEM	CONDITION			STANDARD	NOTE
1	High Temp. Storage	80°C	240 Hrs		Appearance without defect	
2	Low Temp. Storage	-30°C	240 Hrs		Appearance without defect	
3	High Temp. & High Humi. Storage	60°C 90%RH	240 Hrs		Appearance without defect	
4	High Temp. Operating Display	70°C	240 Hrs		Appearance without defect	
5	Low Temp. Operating Display	-20°C	240 Hrs		Appearance without defect	
6	Thermal Shock	-20°C, 30min.	70°C, 30min.	(1cycle)	Appearance without defect	10 cycles

13.Touch Screen Panel Specifications

The non-specified tolerance of dimension is ±0.2mm.

14. Inspection specification

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Missing vertical, horizontal segment, segment contrast defect.
1.2 Missing character, dot or icon.
1.3 Display malfunction.
1.4 No function or no display.
1.5 Current consumption exceeds product specifications.
1.6 LCD viewing angle defect.
1.7 Mixed product types.
1.8 Contrast defect.</td><td>0.65</td></tr>
<tr><td>02</td><td>Black or white spots on LCD (display only)</td><td>2.1 White and black spots on display ≦0.25mm, no more than three white or black spots present.
2.2 Densely spaced: No more than two spots or lines within 3mm</td><td>2.5</td></tr>
<tr><td rowspan="2">03</td><td rowspan="2">LCD black spots, white spots, contaminatio n (non-display)</td><td>3.1 Round type : As folllowing drawing
=(x+y)/2</td><td>2.5</td></tr>
<tr><td>3.2 Line type : (As following drawing)

<table>
<tr><th>Length</th><th>Width</th><th>Acceptable Q TY</th></tr>
<tr><td>---</td><td>W≦0.02</td><td>Accept no dense</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td rowspan="2">2</td></tr>
<tr><td>L≦2.5</td><td>0.03＜W≦0.05</td></tr>
<tr><td>---</td><td>0.05＜W</td><td>As round type</td></tr>
</table></td><td>2.5</td></tr>
<tr><td>04</td><td>Polarizer bubbles</td><td>If bubbles are visible, judge using black spot specification not ease to find, must check in specify direction.
<table>
<tr><th>Size</th><th>Acceptable Q ty</th></tr>
<tr><td>≤0.20</td><td>Accept no dense</td></tr>
<tr><td>0.20＜ ≤0.50</td><td>3</td></tr>
<tr><td>0.50＜ ≤1.00</td><td>2</td></tr>
<tr><td>1.00＜</td><td>0</td></tr>
<tr><td>Total Qty.</td><td>3</td></tr>
</table></td><td></td></tr>
</table>

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>05</td><td>Scratches</td><td>Follow NO.3 LCD black spots, white spots, contamination</td><td></td></tr>
<tr><td>06</td><td>Chipped glass</td><td>
Symbols Define:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: LCD side length
L: Electrode pad length:

6.1 General glass chip :
6.1.1 Chip on panel surface and crack between panels:

<table>
<tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙If there are 2 or more chips, x is total length of each chip.

6.1.2 Corner crack:

<table>
<tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙If there are 2 or more chips, x is the total length of each chip.
</td><td>2.5</td></tr>
</table>

NO	Item	Criterion	AQL
06	Glass crack	Symbols : x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length 6.2 Protrusion over terminal : 6.2.1 Chip on electrode pad :	2.5

y: Chip width	x: Chip length	z: Chip thickness
y≦0.5mm	x≦1/8a	0 ＜ z ≦ t

6.2.2 Non-conductive portion:

y: Chip width	x: Chip length	z: Chip thickness
y≦ L	x≦1/8a	0 ＜ z ≦ t

⊙If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.

⊙If the product will be heat sealed by the customer, the alignment mark not be damaged.

6.2.3 Substrate protuberance and internal crack.

y: width	x: length
y≦1/3L	x ≦ a

NO	Item	Criterion	AQL
07	Cracked glass	The LCD with extensive crack is not acceptable.	2.5
08	Backlight elements	8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using LCD spot, lines and contamination standards. 8.3 Backlight doesn't light or color wrong.	0.65 2.5 0.65
09	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination. 9.2 Bezel must comply with job specifications.	2.5 0.65
10	PCB、COB	10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down. 10.9 The Scraping testing standard for Copper Coating of X Y **X * Y<=2mm²**	2.5 2.5 2.5 0.65 2.5 2.5 0.65 0.65 2.5 2.5
11	Soldering	11.1 No un-melted solder paste may be present on the PCB. 11.2 No cold solder joints, missing solder connections, oxidation or icicle. 11.3 No residue or solder balls on PCB. 11.4 No short circuits in components on PCB.	2.5 2.5 2.5 0.65

NO	Item	Criterion	AQL
12	General appearance	12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP. 12.2 No cracks on interface pin (OLB) of TCP. 12.3 No contamination, solder residue or solder balls on product. 12.4 The IC on the TCP may not be damaged, circuits. 12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it causes the interface pin to sever. 12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color. 12.7 Sealant on top of the ITO circuit has not hardened. 12.8 Pin type must match type in specification sheet. 12.9 LCD pin loose or missing pins. 12.10 Product packaging must the same as specified on packaging specification sheet. 12.11 Product dimension and structure must conform to product specification sheet.	2.5 0.65 2.5 2.5 2.5 2.5 2.5 0.65 0.65 0.65 0.65

15. Precautions in use of LCD Modules

1. Avoid applying excessive shocks to the module or making any alterations or modifications to it.
2. Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
3. Don't disassemble the LCM.
4. Don't operate it above the absolute maximum rating.
5. Don't drop, bend or twist LCM.
6. Soldering: only to the I/O terminals.
7. Storage: please storage in anti-static electricity container and clean environment.
8. Evolute have the right to change the passive components
   (Resistors,capacitors and other passive components will have different appearance and color caused by the different supplier.)
9. Evolute have the right to change the PCB Rev.

16. Material List of Components for RoHs

1. Evolute Solutions Pvt. Ltd. hereby declares that all of or part of products, including, but not limited to, the LCM, accessories or packages, manufactured and/or delivered to your company (including your subsidiaries and affiliated company) directly or indirectly by our company (including our subsidiaries or affiliated companies) do not intentionally contain any of the substances listed in all applicable EU directives and regulations, including the following substances.

   Exhibit A：The Harmful Material List

Material	(Cd)	(Pb)	(Hg)	(Cr6+)	PBBs	PBDEs
Limited Value	100 ppm	1000 ppm	1000 ppm	1000 ppm	1000 ppm	1000 ppm
Above limited value is set up according to RoHS.						

2. Process for RoHS requirement：
   (1) Use the Sn/Ag/Cu soldering surface；the surface of Pb-free solder is rougher than we used before.
   (2) Heat-resistance temp.：
   Reflow：250℃, 30 seconds Max.；
   Connector soldering wave or hand soldering：320℃, 10 seconds max.
   (3) Temp. curve of reflow, max. Temp.：235±5℃；
   Recommended customer's soldering temp. of connector：280℃, 3 seconds.

17. Recommendable storage

1. Place the panel or module in the temperature 25°C±5°C and the humidity below 65% RH
2. Do not place the module near organics solvents or corrosive gases.
3. Do not crush, shake, or jolt the module